📚 Course Outline: 3-Phase Bus Protection Strategies

Module 1: Fundamentals of Substation Bus Protection

- **1.1 Introduction to Busbars and Substation Layouts**
  - Purpose and function of substation busbars.
  - Common bus configurations: **Single Bus-Single Breaker**, **Double Bus-Single Breaker**, **Ring Bus**, and **Breaker-and-a-Half** schemes.
  - Fault types and characteristics on busbars (e.g., three-phase, line-to-ground).
  - The importance of **dependability** (clearing all faults) vs. **security** (avoiding false trips) in bus protection.
- **1.2 Essential Protection Components**
  - **Current Transformers (CTs):** Types, specifications (ratio, accuracy, burden), and saturation concerns during bus faults.
  - **Voltage Transformers (VTs/PTs):** Role in bus protection schemes.
  - **Circuit Breakers (CBs):** Operating principles, trip/close circuits, and clearing times.
  - Introduction to Protective Relays (**Intelligent Electronic Devices - IEDs**).

Module 2: Current-Based Differential Protection Schemes

- **2.1 Principles of Differential Protection (ANSI 87B)**
  - Kirchhoff's Current Law applied to a bus protection zone.
  - The concept of a "zone of protection" and overlapping zones.
  - Setting the operating and restraining characteristics.
- **2.2 High-Impedance Differential Protection**
  - Operating principles and circuit diagrams.
  - Mechanism for securing the scheme against **CT saturation** on external faults.
  - Calculating stabilizing resistors and non-linear resistors (varistors).

  - Applications and limitations.

- **2.3 Low-Impedance Differential Protection (Microprocessor-Based)**
  - Digital implementation: sampling, internal CT ratio matching, and software-based summation.
  - **Percentage Restraint** (Biased Differential) Principle.
  - Techniques for detecting and blocking operation during CT saturation.
  - Application to reconfigurable busbars via **Dynamic Bus Replica** or circuit breaker auxiliary contacts.

Module 3: Non-Differential and Backup Protection

- **3.1 Non-Unit Protection Schemes**
  - **Overcurrent Protection (ANSI 50/51)** as a simple bus backup.
  - Interlocking schemes (e.g., directional/distance relays on feeders acting as bus protection backup).
- **3.2 Breaker Failure Protection (BFP - ANSI 50BF)**
  - The necessity of BFP for bus faults and its role in cascading trip operations.
  - Detection of CB failure (e.g., lack of current interruption after a trip command).
  - Designing the BFP zone and the trip-and-re-trip logic.
- **3.3 Auxiliary and Gas-Insulated Substation (GIS) Protection**
  - **Arc Flash Detection (AFD):** Principles, sensors (light and pressure), and high-speed tripping.
  - GIS-specific issues and protection considerations.

Module 4: Practical Application and Configuration

- **4.1 Protection System Design Considerations**
  - Selecting the appropriate bus protection scheme based on bus configuration (e.g., Ring Bus doesn't typically require a dedicated 87B).

  - Determining the need for **redundancy** (dual independent protection systems).
  - Bus sectioning and zone arrangements.
- **4.2 Current Transformer Sizing and Placement**
  - Sizing CTs for bus differential circuits.
  - Proper CT grounding and polarity checks.
- **4.3 Configuration and Setting Calculations**
  - Step-by-step process for calculating settings for High- and Low-Impedance schemes.
  - Verification of settings for security and dependability.

Module 5: Testing, Commissioning, and Modern Trends

- **5.1 Commissioning and Testing**
  - Secondary injection testing and end-to-end testing of the scheme.
  - Field wiring checks (e.g., CT circuit continuity).
  - Ensuring logic is correct for various operating conditions (breaker open/closed).
- **5.2 Integration with Modern Substation Automation**
  - Using the **IEC 61850** standard for high-speed inter-relay communication (e.g., **GOOSE** messaging).
  - Digital substations and the use of Merging Units.
- **5.3 Troubleshooting and Case Studies**
  - Analyzing event reports and oscillography (**COMTRADE** files) from actual bus faults.
  - Review of common miss-operations (false trips/failures to trip) and remedies.

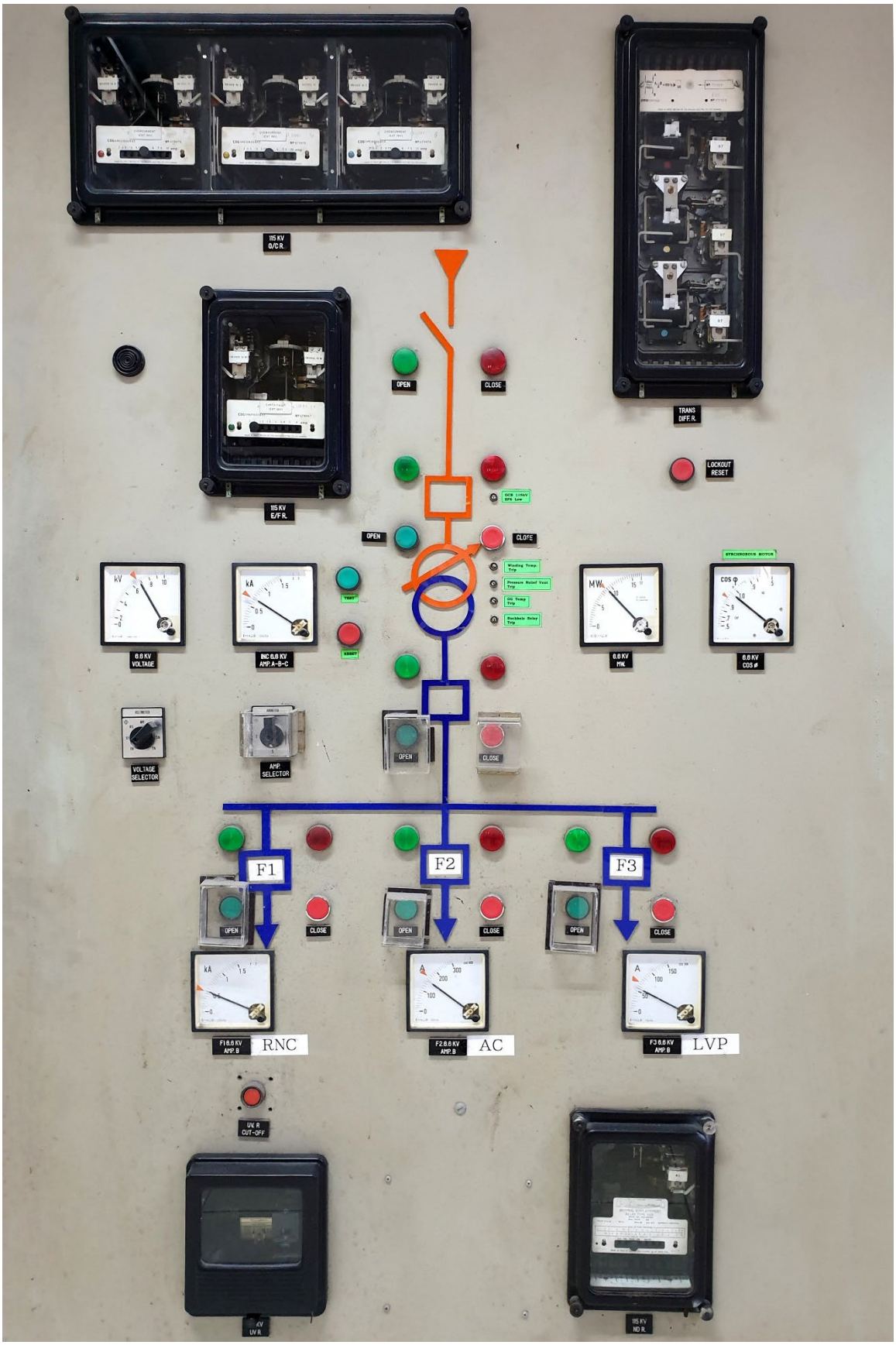
🛠️ **Module 5: Practical SEL Relay Implementation for Bus Protection**

5.1 SEL Bus Protection Relay Hardware Overview

- **Introduction to SEL Relay Platforms:** Focus on devices commonly used for bus protection (e.g., **SEL-487B** or similar SEL differential relays).
- **Front Panel Interface:** Navigation, status LEDs, and accessing event reports.
- **Rear Panel Connections:**
    - Terminal block layouts for **AC Current Inputs** (CT circuits).
    - **Control Power** (DC or AC).
    - **Digital Inputs** (DI) for Breaker Status and Configuration Switches.
    - **Digital Outputs** (DO) for Trip Coils and Alarms.
    - **Communication Ports** (Serial, Ethernet, Fiber).

5.2 Physical Wiring and Termination

- **CT Wiring for Differential Protection:**
    - Proper connection of the current circuits (H1/H2) to ensure **correct polarity**.
    - Importance of using dedicated CT cores for the bus differential relay.
    - Wiring of the **CT Shorting Block** for safety and testing.
- **Control Circuit Wiring:**
    - Wiring the DI's to auxiliary contacts on circuit breakers to implement **Dynamic Bus Replica** logic.
    - Wiring the DO's to the circuit breaker's **Trip Coils**.
- **Grounding and Shielding:** Best practices for relay panel grounding to mitigate **EMI** and ensure security.


115 KV O/C R.
115 KV E/F R.
TRANS DIFF. R.
OPEN
CLOSE
LOCKOUT RESET
8.6 KV VOLTAGE
INC 8.6 KV AMP. A-B-C
8.6 KV MW.
8.6 KV COS ø
VOLTAGE SELECTOR
AMP. SELECTOR
F1
F2
F3
F1 8.6 KV AMP. B
RNC
F2 8.6 KV AMP. B
AC
F3 8.6 KV AMP. B
LVP
UV. R CUT-OFF
KV U/V R.
115 KV 1ID R.

5.3 Relay Configuration and SEL Compass

- **Introduction to SEL's AcSELerator Compass Software:**
  - Connecting to the relay (Serial vs. Ethernet).
  - Downloading and uploading settings files.
  - Creating a new configuration file template.
- **AC Input Setup:**
  - Defining **CT Ratios** (Primary and Secondary).
  - Specifying the connection method (Wye/Delta).
  - Setting nominal AC values.
- **Digital Input (DI) and Output (DO) Configuration:**
  - Assigning names and functions to DIs (e.g., 'BRK52A_CLOSED', 'BUS_A_CONFIG').
  - Configuring DO's for primary and breaker failure tripping.

5.4 Bus Differential Logic and Settings Programming

- **Low-Impedance Differential (87B) Settings:**
  - Setting the **Slope 1 and Slope 2** percentages for the characteristic curve.
  - Defining the **Operating Pickup Threshold** (I_{op}).
  - Setting the **CT Saturation Detection** and transient blocking timers.
- **Configuration Logic Programming:**
  - Implementing the **Breaker-and-a-Half** or **Ring Bus** logic using **SEL's ASCII Logic** (SELogic).
  - Creating the **Bus Differential Logic Equation** using DI's and internal bits to dynamically adjust the zone.
- **Event Reporting and Communications:**
  - Configuring the recording of oscillography (**COMTRADE** records) on trip events.
  - Setting up **DNP3** or **IEC 61850** communications for SCADA integration.

5.5 Testing and Troubleshooting with SEL Tools

- **Testing Procedures:** Using the **SEL Test Set** or equivalent equipment to perform functional tests.
    - **Minimum Trip Test:** Verifying the I_{op} setting.
    - **Slope Test:** Verifying the operating characteristic curve.
    - **DI/DO Checkout:** Verifying the correct operation of all control inputs and outputs.
- **Analyzing Event Reports:** Interpreting **Sequential Events Records (SER)** and oscillography to diagnose a fault or a misoperation.
- **SELogic Troubleshooting:** Using the software's **Live Status** to trace logic execution in real-time.

⚡ Module 6: NEC 240.87 Compliance and Arc Flash Mitigation

- **6.1 Understanding NEC 240.87 (Arc Energy Reduction)**
    - **Scope:** Application to circuit breakers rated **1,200 Amps or higher**.
    - **Core Requirement:** The need to reduce the intentional time delay in clearing a fault to minimize **incident energy**.
    - The relationship between clearing time and incident energy ($IE \propto t$).
- **6.2 Bus Protection Strategies as Arc Flash Mitigation**
    - Review of **Differential Relaying (ANSI 87B)** as a primary compliance method.
        - How instantaneous operation (no intentional delay) inherently satisfies the reduction requirement.
    - **Zone Selective Interlocking (ZSI):**
        - Principle of operation: communication between upstream and downstream protective devices to isolate the fault without intentional time delay.
        - Applying ZSI to a bus feeder/main configuration for faster tripping.
- **6.3 Other Accepted Mitigation Techniques (Per NEC 240.87)**
    - **Energy-Reducing Maintenance Switching (RELT):**

        - Using a temporary reduced energy setting (e.g., lower instantaneous trip) for maintenance.
        - Requirements for a local status indicator.
    - **Energy-Reducing Arc Flash Mitigation Systems (Light/Pressure Sensors):**
        - Using sensors (optical/fiber-optic) to detect arc flash light/pressure for near-instantaneous tripping.
        - Integration with the main bus protection relay (e.g., SEL-487B Arc-Flash module).
    - **Instantaneous Override:** Using a lower instantaneous trip setting than the available arcing current.
- **6.4 Coordination Studies and Compliance Verification**
    - **Time-Current Curve (TCC) Analysis:** Demonstrating how the chosen mitigation method reduces the fault clearing time on the TCC.
    - **Arc Flash Study:** Calculation of incident energy (cal/cm^2) before and after implementation of the mitigation strategy.
    - **Documentation:** Providing records to the **Authority Having Jurisdiction (AHJ)** to prove compliance.